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A four channel, self-calibrating, high resolution, Time To Digital Converter.

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Abstract.

A four channel, self-calibrating, High Resolution Time to Digital Converter (HRTDC) with an RMS error of 35 ps over a dynamic range of 3.2 μs has been developed. Its architecture is based on an array of delay locked loops and an 8-bit coarse time counter driven by an 80 MHz reference clock. Time measurements are buffered in two time registers per channel followed by a common 32 words deep read-out FIFO. The HRTDC has been built in a 0.7 μm CMOS process using 23 mm^2 of silicon area.

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A four channel, self-calibrating, High Resolution Time to Digital Converter (HRTDC) with an RMS error of 35 ps over a dynamic range of 3.2 μs has been developed. Its architecture is based on an array of delay locked loops and an 8-bit coarse time counter driven by an 80 MHz reference clock. Time measurements are buffered in two time registers per channel followed by a common 32 words deep read-out FIFO. The HRTDC has been built in a 0.7 μm CMOS process using 23 mm^2 of silicon area.

1. Introduction.

High Energy Physics experiments require high resolution time measurements on a very large number (~10^5) of detector channels. The time resolution needed for measuring the flight time of particles ranges from 10 ps to 100 ps RMS over a limited dynamic range. Extended dynamic range is however useful at the system level to time tag events for future off-line analysis.

Traditionally time measurements have been performed using time to amplitude converters followed by an ADC [1]. These converters can achieve the resolution required but are not easy to integrate into a single IC and usually feature small dynamic range. Issues such as temperature stability, supply voltage sensitivity and linearity are often problematic for these devices.

In this paper, a High Resolution TDC (HRTDC) developed to serve the needs of detectors such as the ALICE Pestov spark counter [2] will be described. This detector requires precise time measurements on ~380,000 channels in a highly integrated environment.

2. HRTDC Architecture.

The converter architecture can be divided into two main building blocks (see *Fig. 1*): In the timing core an array of Delay Locked Loops (DLL) performs time interpolation within a period of the reference clock (fine time). A clock synchronous counter is used to obtain a larger dynamic range (coarse time). Measurements are stored in two levels of temporary asynchronous channel buffer.

In the read-out and logic block, the data stored in the channel buffers are multiplexed into a single data stream. The status of the array (fine time) is converted into a binary code and the correct coarse time is selected. These data (fine and coarse time, channel id, status flags) are then stored as a single word in the read-out FIFO.

By using a common derandomizer FIFO to gather data from all channels, the channel buffers can be freed to acquire new hits. This buffering architecture, with small buffers per channel and a common derandomizer is very efficient in terms of occupied area and small dead time.

3. Timing core.

An array of DLLs is at the core of the architecture implemented. DLL-based architectures have several features that make them very attractive for this application [3]: The closed control loop guarantees permanent self-calibration, making the converter insensitive to voltage and temperature changes. It can be produced in a standard CMOS technology, with a high level of integration and thus lower system costs. The converter's dynamic range can be expanded simply by including a coarse counter, counting reference clock cycles.

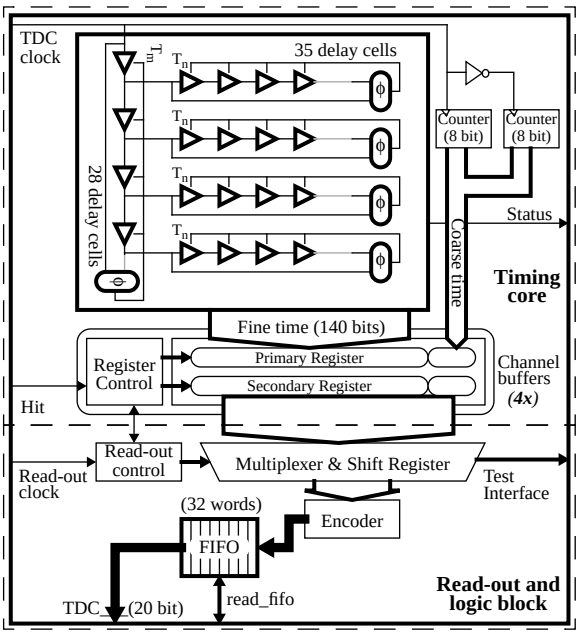

Fig. 1. HRTDC block diagram.

In a DLL (see *Fig. 2*) the reference clock is propagated through a voltage controlled delay line. The delay of the signal arriving at the end of the line is compared with the

delay at the beginning. If a delay difference other than one clock period is detected, the closed loop will correct it by changing the time constant of the delay cells via a charge pump and filter capacitor. An initialization state-machine forces the loop to lock to a delay difference of one clock period, avoiding false locks to multiples of clock periods (or to zero delay).

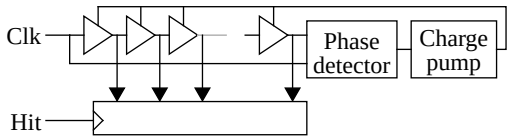

Fig. 2. DLL block diagram.

The arrival time of a hit signal is measured relative to the reference clock, resulting in a "time-stamp" measurement [4],[5]. "Start-stop" measurements can be obtained if a second channel is used to store the start value, which is then subtracted from the stop measurement.

A single DLL has a time resolution limited to the basic cell delay (T_n). The resolution can be improved F times ($F > 1$) by using an array of DLLs [5], In this scheme a small phase shift between F consecutive DLLs is used to obtain a bin size that is a fraction $F^{-1} \cdot T_n$ of the gate delay.

Such a small delay cannot be obtained directly. It is, however, possible to generate a delay of $1 + F^{-1}$ times the basic delay cell. This is done using an additional phase shifting DLL, with a smaller number (M) of delay elements than the other DLLs in the array (N delay elements each), locked to the same reference.

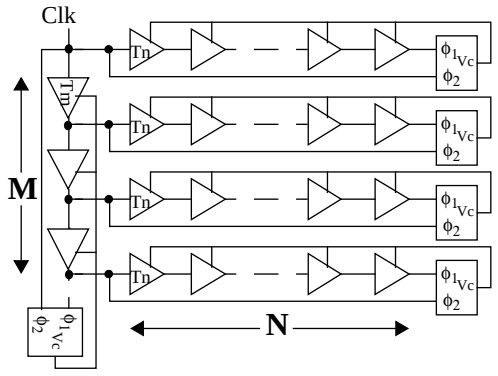

Fig. 3. DLL array with Phase Shifting DLL.

An arrangement such as this (*Fig. 3*) results in a delay of $(1 + F^{-1}) \cdot T_n$ between corresponding taps in consecutive DLLs. Due to the symmetry of the array, one cell delay can easily be subtracted, resulting in a delay between consecutive taps that is only $F^{-1} \cdot T_n$.

The time bins are obtained from small time differences of accumulated delays in consecutive DLLs. Any error in these delays will be amplified by the nature of the interpolation and will severely degrade the linearity of the converter. It is therefore essential to obtain good matching characteristics between devices throughout the time critical paths.

Unfortunately the array scheme is unable to produce a number of bins that is a power of 2. This results in a fine time word that is coded in a $N \cdot F$ base and not in the usual 2^b binary code (where b is the number of bits). However conversion to normal binary code can easily be performed off-line.

Since all DLLs are locked to the same reference, dynamic range extension is easily achieved by introducing a coarse counter that counts reference clock cycles. In order to avoid metastability due to the sampling of the counter's outputs, close to their transition, two counters synchronous to opposite phases of the reference clock are used. Selection of the correct value is done in accordance with the relative position of the hit arrival within the clock period, as given by the fine time (*Fig. 4*).

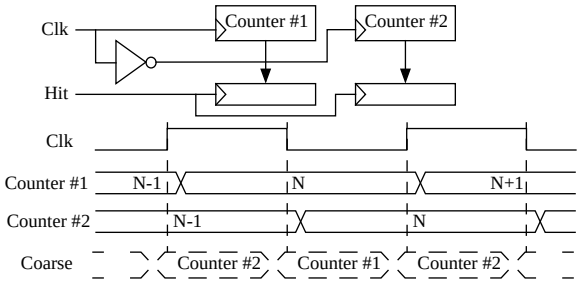

Fig. 4. Coarse Time selection.

The time information stored in a channel buffer contains the status of the array and of the coarse time counters. In order to minimize dead-time between measurements, the architecture includes a small buffer per channel, controlled via an asynchronous state machine.

4. Implementation Issues.

Two main criteria drove the design effort of the time critical circuitry of the converter: matching and noise immunity. They are reflected in the topologies chosen for the circuitry. In the following the implementation of the most important circuits is discussed.

4.1 Delay cells.

A delay cell is schematically drawn in *Fig. 5*. It is made of two current-starved inverters. Separate buffering of the outputs driving the channel buffers and the phase detector (*tapA_b* and *tapB_b*) are required to maintain correct path delay matching.

Differential delay cell topologies were also evaluated due to their apparent noise immunity. Unfortunately a completely differential control loop is difficult to obtain, limiting the high frequency noise immunity. Simulations where fast changes in power supply levels (supply noise) are applied have not shown a significant advantage for the differential configuration. Also differential cells increase power consumption.

In a DLL the delay cells are deliberately slowed down and their switching is evenly distributed over the clock period. Power supply noise generated by the DLL is thus minimized.

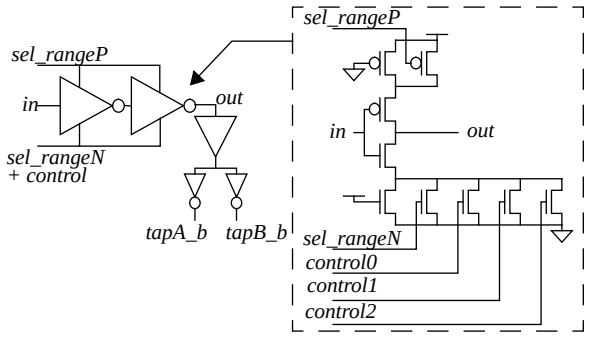

Fig. 5. Delay cell and detail of one current starved inverter.

Matching[1] between devices is both dependent on technology and design parameters [6]. It is proportional to the $\sqrt{(gate\ area)}$ and also depends on the operating point of the device. All critical devices were designed with gate areas large enough to guarantee an acceptable level of matching.

To maintain the matching characteristics in any process and environment conditions, the delay control transfer curve was divided in several partially overlapping ranges. The corresponding loop gain is determined by a programmable bias current (signals *sel_rangeN* and *sel_rangeP* in *Fig. 5*) and by the connection of one or more current-starved transistors to the control voltage generated in the charge pump (signals *control0...2*). In this way it is always possible to obtain lock in an operating point that is favourable in terms of matching. An added advantage of this scheme is a reduced noise sensitivity due to the smaller cell gain (slope of the control voltage-cell delay transfer curve in *Fig. 6*), for any selected range.

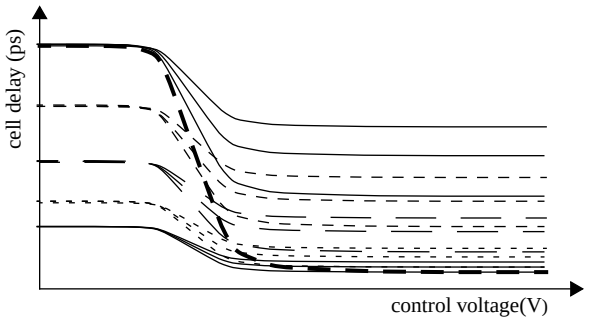

Fig. 6. Delay cell control curve, with range sub-divisions.

Fig. 6 shows the delay of each delay cell as a function of the voltage on the filter capacitor (determined by the closed control loop). Each curve represents one slope-offset selection. They partially overlap to avoid the existence of any dead region between curves and to make the selection of the working range easier.

With this topology, the circuit can acquire lock in any process or environment conditions. Lock can be maintained over variations of $\pm 15^{o}$ C in temperature and $\pm 300\ mV$ in power supply. This is considered sufficient for the controlled environment where the circuit will work.

4.2 Phase detector.

The phase detector (PD) samples the status of the last tap in the DLL at the instant a rising edge of the reference enters the DLL. A basic D flip-flop can, in principle, be used to perform this task. The loop is then controlled using a "bang-bang" configuration.

Standard D flip-flops usually display different setup and hold times, and a badly defined sampling time. This may result in a significant static phase error. A thoroughly balanced design (*Fig. 7* [7]), and good device matching characteristics are therefore required to ensure minimal static phase error.

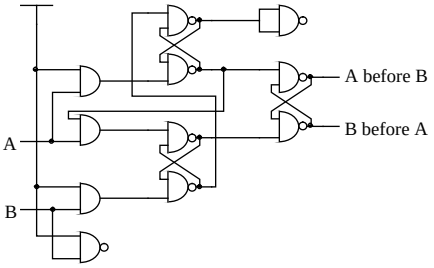

Fig. 7. Phase Detector using balanced D-flip-flop.

The delay of signals to the PD must also match very closely, due to their direct contribution to the phase error. For the time resolution required, distributed parasitic RC models of signal wires must be used to evaluate and minimize these potential skews.

4.3 Input signal integrity, noise avoidance.

In contrast to a PLL, a DLL is unable to filter jitter present on the reference clock. To obtain the high-resolution required, special care must therefore be taken to ensure that the handling of the critical signals (reference clock, but also hit inputs) do not compromise the required resolution. Differential signalling levels have therefore been used for these input signals.

Inside the circuit, special care has been taken to avoid coupling between the potentially noisy digital read-out block and time-critical DLLs via the power supply or the common substrate. Separate power supplies and careful use of guard-rings minimizes noise coupling.

5. Demonstrator.

A demonstrator circuit was designed in a 0.7 μm CMOS technology. The main performance design goal was a res-

1. The time independent random variations in physical quantities of identically designed devices is called *device mismatch* [6]. These variations result in having identical devices with different electrical characteristics.

olution better than 50 ps RMS across the 3.2 μs dynamic range.

An 80 MHz reference clock is propagated through four (F= 4) timing DLLs made of 35 delay elements (N = 35) and a phase shifting DLL with only 28 delay elements (M = 28). This configuration results in an effective bin size of $T_{clk}/(N \cdot F)$ = $12.5ns/140$ = $89.3ps$ and a theoretical resolution of $89.3ps/\sqrt{12}$ = $25.8ps$ (RMS). Matching limitations and jitter associated with the reference and the closed loop were estimated to contribute with a σ of ~15ps, degrading the expected resolution to ~30ps. An 8-bit coarse time counter was used for dynamic range expansion.

Characterization of the converter's Differential and Integral Non-Linearities (DNL and INL, respectively) was performed using Statistical Code Density Tests, from a data set of 840,000 random hits. The resulting histograms are shown in *Fig. 8*. The converter's DNL was measured to have σ= 12.8 ps (0.14 LSB) and its INL to have σ= 15.3 ps (0.17 LSB).

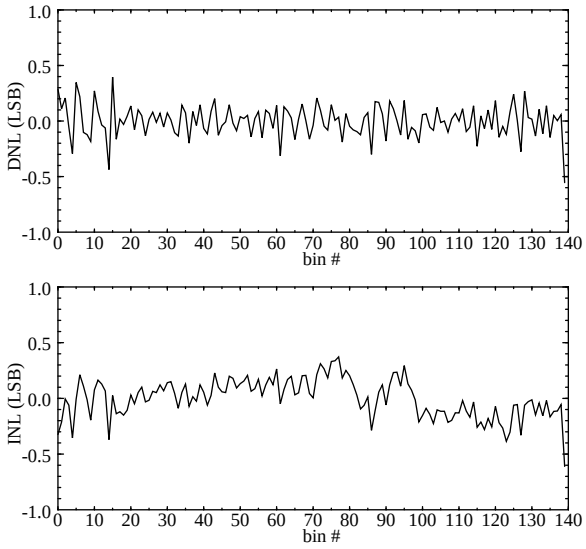

Fig. 8. DNL and INL histograms of the array.

A Linear Time Sweep over the dynamic range was performed in order to measure errors of random nature such as jitter, internal and external noise, etc. These kind of errors are not captured by statistical tests, due to their random behaviour.

A motor-driven coaxial phase shifter was used to generate a time sweep. This passive instrument is very linear and generates very little jitter, so it is better suited for this application than active delay generators. Using this setup, the RMS resolution of the converter was measured to be 34.3ps (0.38 LSB), with a maximum error smaller than ±1.2 bins (107 ps). The plot in *Fig. 9* shows the conversion error histogram. It includes 60,000 measurements generated with a time step of ~2.8 ps (accumulating 5 measures per time step).Another important parameter of a multi-channel TDC is the crosstalk between channels. It has been measured to be smaller than ±2 bins in any condition.

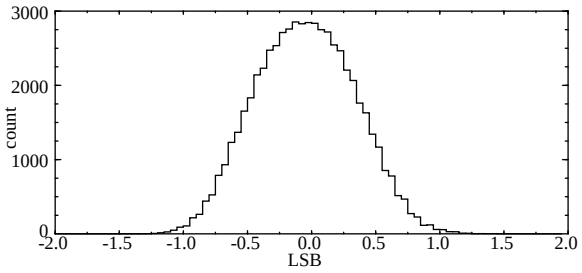

Fig. 9. Conversion error histogram (σ= 0.38 LSB)

The following table shows the most important characteristics of the HRTDC:

Timing characteristics:	
resolution:	34.3ps (RMS).
dynamic range:	3.2 μs.
reference clock frequency:	80 MHz.
bin size (LSB):	89.3 ps.
DNL (σ / max):	0.14 / 0.55 LSB.
INL (σ / max):	0.17 / 0.61 LSB.
crosstalk:	< ±2 bin.
Functional characteristics:	
n^{o}. of channels:	4.
power consumption:	800 mW.
reference clock logic levels:	differential PECL.
hit inputs logic levels:	differential PECL.
buffer depth (Read-out FIFO):	32 word.
buffer depth (hit registers):	2 word/channel.
output word length:	20 bits.
silicon area:	23 mm^2.
package	68 pins PLCC.

6. Conclusions.

A High-Resolution TDC converter based on a DLL array has been described. A prototype was produced to validate the proposed architecture. It showed that it is possible to obtain RMS resolutions better than 50 ps across a large dynamic range in a multi-channel monolithic circuit. Since a standard CMOS technology was used, it was possible to integrate memory and logic, enhancing the circuit's functionality without degrading its performance.

7. Acknowledgment.

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